CLAIM LISTING

The claims as listed in this claim listing replace all previous versions of the claims.

1. **(Currently Amended)** A method comprising:

initializing a ~~circuit said~~ **circuit, the** circuit having at least one memory element coupled to a memory bus on a host system;

monitoring signals on the memory bus;

detecting a ~~first~~ sequence of signals **in response to monitoring,** the ~~first~~ sequence of signals including a reserved memory address; and

switching control of the ~~at least one~~ memory element to **one of** the circuit **and the host system** in response to detection of the reserved memory address.

2. **(Currently Amended)** The method of claim 1 ~~further comprising:~~ **wherein** detecting ~~a second~~ **the** sequence of signals**[[, the]] further comprises detecting a first sequence of signals including a first reserved memory address and detecting a** second sequence of signals including ~~another~~ **a second** reserved memory address**[[;]]** and **wherein** switching control of the ~~at least one~~ memory element **comprises switching control to the circuit in response to detection of the first reserved memory address, and switching control** to the host system in response to detection of the ~~another~~ **second** reserved memory address.

3. (Original) The method of claim 2 wherein error correcting codes are switched off prior to switching control of the at least one memory element to the host system.

4. (Original) The method of claim 1 wherein initializing a circuit having at least one memory element coupled to a memory bus on a host system comprises detecting a sequence of writes to memory locations on the circuit.

5. (Original) The method of claim 4 wherein the sequence of writes are writes to random memory locations on the circuit.

6. (Original) The method of claim 1 wherein monitoring signals on the memory bus comprises the circuit monitoring control, address, and data signals on the host system.

7. (Previously Presented) The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one write signal to the reserved memory address.

8. (Previously Presented) The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one read signal from the reserved memory address.

9. (Previously Presented) The method of claim 1 wherein switching control of the memory bus to the circuit comprises a processing element in the circuit reading from or writing to the at least one memory element in the circuit.

10. (Original) The method of claim 2 wherein switching control of the at least one memory element to the host system comprises a processor on the host system reading from or writing to the at least one memory element.

11. (**Currently Amended**) An apparatus comprising:

a memory bus on a host system;

a plurality of memory elements on a circuit, said plurality of memory elements communicatively coupled with the memory bus;

a processing element on the circuit communicatively coupled with the plurality of memory elements and the memory bus, said processing element to

monitor signals on the memory bus;

detect a ~~first~~ sequence of signals **in response to monitoring**, the ~~first~~ sequence of signals including a reserved memory address; and

switch control of the plurality of memory element to **one of** the circuit **and the host system** in response to detection of the reserved memory address.

12. **(Currently Amended)** The apparatus of claim 11 ~~**further comprising said**~~ **the** processing element to detect ~~**a second**~~ **the** sequence of signals**[[, the]]** **further comprises the processing element to detect a first sequence of signals including a first reserved memory address and detecting a** second sequence of signals including ~~**another**~~ **a second** reserved memory address; and

switch control of the plurality of memory elements to **the circuit in response to detection of the first reserved memory address and to** the host system in response to detection of the ~~**another**~~ **second** reserved memory address.

13. (Original) The apparatus of claim 12 wherein error correcting codes are switched off prior to switching control of the plurality of memory element to the host system.

14. (Original) The apparatus of claim 11 wherein the processing element is at least one of a field programmable gate array, and a processor.

15. (Original) The apparatus of claim 11 wherein the processing element to monitor signals on the memory bus comprises the processing element to monitor control, address, and data signals on the host system.

16. (Previously Presented) The apparatus of claim 11 wherein the processing element to detect a first sequence of signals comprises the processing element to detect at least one write signal to the reserved memory address.

17. (Previously Presented) The apparatus of claim 11 wherein the processing element to detect a first sequence of signals comprises the processing element to detect at least one read signal to the reserved memory address.

18. (Original) The apparatus of claim 11 wherein the processing element to switch control of the plurality of memory element to the circuit comprises the processing element reading from or writing to the plurality of memory elements.

19. (Original) The apparatus of claim 12 wherein the processing element to switch control of the plurality of memory elements to the circuit comprises a processor on the host system reading from or writing to the plurality of memory elements.

20. **(Currently Amended)** An article of manufacture comprising:

a machine-accessible medium including instructions that, when executed by a machine, causes the machine to perform operations comprising

initializing a ~~**circuit said**~~ **circuit, the** circuit having at least one memory element coupled to a memory bus on a host system;

monitoring signals on the memory bus;

detecting a ~~**first**~~ sequence of signals **in response to monitoring**, the ~~**first**~~ sequence of signals including a reserved memory address; and

switching control of the ~~**at least one**~~ memory element to **one of** the circuit **and the host system** in response to detection of the reserved memory address.

21. **(Currently Amended)** The article of manufacture as in claim 20, ~~**further comprising**~~ **wherein the** instructions for detecting ~~**a second**~~ **the** sequence of signals**[[, the]]** **comprise instructions for detecting a first sequence of signals including a first reserved memory address and detecting a** second sequence of signals including ~~**another**~~ **a second** reserved memory address; and

switching control of the ~~at least one~~ memory element to **the circuit in response to detection of the first reserved memory address and to** the host system in response to detection of the ~~another~~ **second** reserved memory address.

22. (Original) The article of manufacture as in claim 21, further comprising instructions for switching of error correcting codes prior to switching control of the at least one memory element to the host system.

23. (Original) The article of manufacture as in claim 20, wherein said instructions for initializing a circuit having at least one memory element coupled to a memory bus on a host system comprises further instructions for detecting a sequence of writes to memory locations on the circuit.

24. (Original) The article of manufacture as in claim 23, wherein said instructions for detecting a sequence of writes include further instructions for writing to random memory locations on a circuit.

25. (Original) The article of manufacture as in claim 20, wherein said instructions for monitoring signals on the memory bus comprises further instructions for the circuit monitoring control, address, and data signals on the host system.

26. (Previously Presented) The article of manufacture as in claim 20, wherein said instructions for detecting a first sequence of signals comprises further instructions for detecting at least one write signal to the reserved memory address.

27. (Previously Presented) The article of manufacture as in claim 20, wherein said instructions for detecting a first sequence of signals comprises further instructions for detecting at least one read signal from the reserved memory address.

28. (Previously Presented) The article of manufacture as in claim 20, wherein said instructions for switching control of the memory bus to the circuit comprises further instructions for a processing element in the circuit reading from or writing to the at least one memory element in the circuit.

29. (Original) The article of manufacture as in claim 21, wherein said instructions for switching control of the at least one memory element to the host system comprises further instructions for a processor on the host system reading from or writing to the at least one memory element

30. (Previously Presented) The method of claim 1, wherein the reserved memory address corresponds to a reserved address in the at least one memory element in the circuit.

31. (Previously Presented) The method of claim 1, wherein the reserved memory address corresponds to a reserved address in a second memory coupled with the memory bus.

32. (Previously Presented) The apparatus of claim 11, wherein the reserved memory address corresponds to a reserved address in the plurality of memory elements of the circuit.

33. (Previously Presented) The apparatus of claim 11, wherein the reserved memory address corresponds to a reserved address in a second memory coupled with the memory bus.

34. (Previously Presented) The article of manufacture of claim 20, wherein the reserved memory address corresponds to a reserved address in the at least one memory element in the circuit.

35. (Previously Presented) The article of manufacture of claim 20, wherein the reserved memory address corresponds to a reserved address in a second memory coupled with the memory bus.

36. (Previously Presented) A method comprising:

monitoring signals on a memory bus, the memory bus coupled with a memory and a first processor; and

in response to detecting a reserved memory address on the memory bus, switching control of the memory from the first processor to a second processor coupled with the memory bus.

37. (Previously Presented) The method of claim 36, further comprising:

in response to detecting another reserved memory address on the memory bus, switching control of the memory from the second processor to the first processor.

38. (Previously Presented) The method of claim 36, wherein the reserved memory address corresponds to a reserved address in the memory.

39. (Previously Presented) The method of claim 36, wherein the reserved memory address corresponds to a reserved address in a second memory coupled with the memory bus.

40. (Previously Presented) The method of claim 36, wherein detecting the reserved memory address comprises detecting one of a read to the reserved memory address and a write to the reserved memory address.

41. (Previously Presented) The method of claim 36, wherein the memory and the second processor comprise part of a single component.

42. (Previously Presented) The method of claim 41, wherein the single component comprises a dual inline memory module (DIMM) coupled with the memory bus.

43. (Previously Presented) The method of claim 36, wherein the memory comprises a synchronous dynamic random access memory (SDRAM).

44. **(New)** An apparatus comprising:

a memory element directly coupled to a local memory bus, the local memory bus separate from the system memory bus, the memory element to be addressable via the system memory bus;

an on-board processor having an arbiter to arbitrate the system memory bus, including monitoring the system memory bus for a reserved memory address and issuing a control signal; and

a switch coupled to the local memory bus, the on-board processor, and the system memory bus, to receive the control signal and selectively switch the local memory bus, in response to the control signal, to the on-board processor to switch control of the memory element to the on-board processor, and to the system memory bus to switch control of the memory element to the host system.

45. **(New)** The apparatus of claim 44, wherein the switch to switch the local memory bus to the system memory bus further comprises the switch to interconnect the local memory bus to the host system via one of multiple system memory card slots.

46. **(New)** The apparatus of claim 45, wherein the switch to interconnect the local memory bus to the host system via one of the multiple system memory card slots comprises the apparatus to occupy a dual inline memory module (DIMM) slot, and the switch to interconnect the local memory bus to interconnect pins of the DIMM slot.

47. **(New)** The apparatus of claim 44, wherein the selectively switch the local memory bus comprises the switch, by default, to switch the local memory bus to the system memory bus.

48. **(New)** The apparatus of claim 44, further comprising the on-board processor to perform processing on data from the memory element if the local memory bus is switched to the on-board processor.

49. **(New)** The apparatus of claim 48, wherein the on-board processor to perform processing comprises the on-board processor to perform hardware acceleration of a computationally intensive task to be performed on data in the memory element.

50. **(New)** The apparatus of claim 48, wherein the on-board processor to perform processing comprises the on-board processor to perform processing on data from the memory element concurrently with a processor on the host system performing processing.